#5 Supp IDS w/refs Smw 7-19-01

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Azadet 10-2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Kameran Azadet, Erich Franz Haratsch
Case:	10-2
Serial No.:	09/471,920
Filing Date:	December 23, 1999
Group:	2739
Examiner:	L. Fletcher

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

Signature [signature] Date: July 17, 2001

Title: Method and Apparatus for Shortening the Critical Path of Reduced Complexity Sequence Estimation Techniques

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant's attorney wishes to bring to the attention of the Patent and Trademark Office the following documents listed on the accompanying PTO Form 1449. Copies of the listed items are enclosed.

U.S. Patents:

1. United States Patent No. 5,870,433 to Huber et al.
2. United States Patent No. 6,035,006 to Matui
3. United States Patent No. 6,201,831 to Agazzi et al.

Other Documents:

4. Keshab K. Parhi, "Pipelining in Algorithms with Quantizer Loops," IEEE Transactions on Circuits and Systems, Vol. 38. No. 7, 745-754 (July 1991)
5. Bednarz et al., "Design, Performance, and Extensions of the RAM-DFE Architecture," IEEE Transactions on Magnetics, Vol. 31, No. 2, 1196-1201 (March 1995)

The filing of this Supplemental Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,

Kevin M. Mason

Date: July 17, 2001

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